WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a mask material on a silicon layer on a surface of a semiconductor substrate;

patterning the silicon layer with the mask material used as a mask so as to form a fin-type silicon layer having the mask material formed on the surface;

forming a gate insulating film on side surfaces of the fin-type silicon layer;

depositing a gate material on an entire surface;

patterning the gate material layer so as to form a gate electrode;

introducing an impurity into the fin-type silicon layer with the gate electrode used as mask so as to form first impurity regions;

etching the gate electrode so as to form a gate electrode having a reduced size; and

introducing an impurity into the fin-type silicon layer with the gate electrode of the reduced size used as a mask so as to form second impurity regions positioned adjacent to the first impurity diffusion regions.

2. The method according to claim 1, wherein an etching amount of the gate electrode is not larger than the thickness of the mask material layer.

3. The method according to claim 1, wherein an impurity concentration in the first impurity region is higher than that in the second impurity region.

4. A method of manufacturing a semiconductor device, comprising:

forming a mask material on a silicon layer on a surface of a semiconductor substrate;

patterning the silicon layer with the mask material used as a mask so as to form a fin-type silicon layer having the mask material formed on the surface;

forming a gate insulating film on side surfaces of the fin-type silicon layer;

depositing a gate material on an entire surface;

planarizing the gate material so as to expose the mask material to outside;

patterning the gate material layer so as to form a gate electrode;

introducing an impurity into the fin-type silicon layer with the gate electrode used as mask so as to form first impurity regions;

etching the gate electrode so as to form a gate electrode having a reduced size; and

introducing an impurity into the fin-type silicon layer with the gate electrode of the reduced size used as a mask so as to form second impurity regions positioned adjacent to the first impurity diffusion

regions.

5. A method of manufacturing a semiconductor device, comprising:

forming a mask material on a silicon layer on a surface of a semiconductor substrate;

patterning the silicon layer with the mask material used as a mask so as to form a fin-type silicon layer having the mask material formed on the surface;

forming a gate insulating film on the side surface of the fin-type silicon layer;

depositing a gate material on the entire surface;

planarizing the gate material so as to expose the mask material to the outside;

depositing a second gate material on the entire surface;

patterning the first and second gate material layers so as to form a gate electrode;

introducing an impurity into the fin-type silicon layer with the gate electrode used as a mask so as to form first impurity regions;

etching the gate electrode so as to form a gate electrode having a reduced size; and

introducing an impurity into the fin-type silicon layer with the gate electrode of the reduced size used as a mask so as to form second impurity regions positioned adjacent to the first impurity diffusion

regions.

6. A method of manufacturing a semiconductor device, comprising:

forming a mask material on a silicon layer on a surface of a semiconductor substrate;

patterning the silicon layer with the mask material used as a mask so as to form a fin-type silicon layer having the mask material formed on the surface;

forming a buffer layer on side surfaces of the fin-type silicon layer;

forming a dummy gate material on an entire surface;

planarizing the dummy gate material layer so as to expose the mask material layer to outside;

patterning the dummy gate material layer so as to form a dummy gate;

introducing an impurity into the fin-type silicon layer with the dummy gate used as a mask so as to form first impurity regions;

etching the dummy gate so as to form a dummy gate having a reduced size;

introducing an impurity into the fin-type silicon layer with the dummy gate having a reduced size used as a mask so as to form second impurity regions positioned adjacent to the first impurity regions;

forming an interlayer insulating film on an entire

surface;

planarizing a surface of the interlayer insulating film so as to expose the dummy gate;

removing the dummy gate and the buffer layer so as to form a gate groove;

forming a gate insulating film on an inner surface of the gate groove; and

forming a gate electrode within the gate groove.

7. A method of manufacturing a semiconductor device, comprising:

forming a mask material on a silicon layer on a surface of a semiconductor substrate;

patterning the silicon layer with the mask material used as a mask so as to form a fin-type silicon layer having the mask material formed on the surface;

forming a buffer layer on side surfaces of the fin-type silicon layer;

depositing a first dummy gate material on an entire surface;

planarizing the first dummy gate material layer so as to expose the mask material layer to outside;

depositing a second dummy gate material on an entire surface;

patterning the first and second dummy gate material layers so as to form a dummy gate;

introducing an impurity into the fin-type silicon

layer with the dummy gate used as a mask so as to form first impurity regions;

etching the dummy gate so as to form a dummy gate having a reduced size;

introducing an impurity into the fin-type silicon layer with the dummy gate having a reduced size used as a mask so as to form second impurity regions positioned adjacent to the first impurity regions;

forming an interlayer insulating film on an entire surface;

planarizing a surface of the interlayer insulating film so as to expose the dummy gate;

removing the dummy gate and the buffer layer so as to form a gate groove;

forming a gate insulating film on an inner surface of the gate groove; and

forming a gate electrode within the gate groove.

8. The method according to claim 7, wherein the etching amount of the dummy gate is not larger than the thickness of the mask material layer.

9. A semiconductor device, comprising:

a fin-type silicon layer formed on a semiconductor substrate;

a mask material formed on the fin-type silicon layer;

a gate insulating film and a gate electrode formed in contact with side surfaces of the fin-type silicon

layer and the mask material;

first impurity regions formed a prescribed distance apart from a region corresponding to the gate electrode of the fin-type silicon layer; and

second impurity regions formed between the first impurity regions of the fin-type silicon layer and the region corresponding to the gate electrode.

10. The semiconductor device according to claim 9, wherein the width of the second impurity region is smaller than the thickness of the mask material.

11. The semiconductor device according to claim 9, wherein an impurity concentration in the second impurity region is higher than that in the first impurity region.

12. The semiconductor device according to claim 9, wherein the gate electrode comprises a metal or a metal silicide.

13. The semiconductor device according to claim 9, wherein an impurity concentration in the first impurity region is higher than that in the second impurity region.

14. A semiconductor device, comprising:

a fin-type silicon layer formed on a semiconductor substrate;

a gate insulating film and a gate electrode formed in contact with side surfaces and an upper surface of the fin-type silicon layer;

first impurity regions formed a prescribed distance apart from a region corresponding to the gate electrode of the fin-type silicon layer; and

second impurity regions formed between the first impurity regions of the fin-type silicon layer and the region corresponding to the gate electrode.

15. A semiconductor device, comprising:

a fin-type silicon layer formed on a semiconductor substrate and having first and second side surfaces;

a mask material formed on the fin-type silicon layer;

a first gate insulating film and a first gate electrode formed in contact with the first side surface of the fin-type silicon layer;

a second gate insulating film and a second gate electrode formed in contact with the second side surface of the fin-type silicon layer;

first impurity regions formed a prescribed distance apart from a region corresponding to the first and second gate electrodes of the fin-type silicon layer; and

second impurity regions formed between the first impurity regions of the fin-type silicon layer and the region corresponding to the first and second gate electrodes.

16. A semiconductor device, comprising:

a fin-type silicon layer formed on a semiconductor

substrate and having first and second side surfaces;

a mask material formed on the fin-type silicon layer;

a first gate insulating film and a first gate electrode formed in contact with the first side surface of the fin-type silicon layer;

a second gate insulating film and a second gate electrode formed in contact with the second side surface of the fin-type silicon layer;

a third gate electrode formed in contact with an upper surfaces of the first gate electrode and the second gate electrode;

first impurity regions formed a prescribed distance apart from a region corresponding to the first, second and third gate electrodes of the fin-type silicon layer; and

second impurity regions formed between the first impurity regions of the fin-type silicon layer and the region corresponding to the first, second and third gate electrodes.

17. The semiconductor device according to claim 16, wherein each of the first, second and third gate electrodes comprises a material containing as a main component polycrystalline silicon or amorphous silicon.

18. The semiconductor device according to claim 16, wherein a width of the third gate electrode

is larger than a width of each of the first and second gate electrodes.

19. The semiconductor device according to claim 16, wherein each of the first and second gate electrodes comprises a material containing as a main component polycrystalline silicon or amorphous silicon, and the third gate electrode comprises a metal or a metal silicide.

20. The semiconductor device according to claim 16, wherein each of the first, second and third gate electrodes comprises a material containing as a main component a metal or a metal silicide.